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Gregory W. Osterloth
Holland & Hart, LLP
P.O. Box 8749
Denver, CO 80201

EXAMINER	
CHUNG, PHUNG M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/666,024
Filing Date: September 18, 2003
Appellant(s): HAYHOW, REID

Reid Hayhow
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/18/08 appealing from the Office action mailed 1/31/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,574,626 Regelman et al 6-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes, Jr. (4,493,079) in view of Regelman et al (6,574,626).

As per claim 1, Hughes, Jr. discloses a method comprising: reading a test file including a plurality of test vectors to be applied to a device. (See col. 3, lines 51-61). Hughes, Jr. does not disclose determining a required memory needed to execute the plurality of test vectors. However, Regelman et al discloses the process allocates space in a primary memory for the called pattern and the dependencies. The called pattern and the dependencies are then selectively copied from the secondary memory to the primary memory prior to executing the called pattern (see col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5) is to determine a required memory needed to execute a plurality of test vectors or making sure there is a significant amount of memory needed to execute a plurality of test vectors. Regelman also disclose that the

memory management process determines if there is sufficient room in the primary memory to copy the additional software units such as the new called test pattern and any additional algorithmic subroutines. (See col. 15, lines 50-67 to col. 16, lines 1-10, col. 19, lines 47-67 to col. 20 lines 1-27). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the step of determining a required memory needed to execute the plurality of test vectors as taught by Regelman et al into the invention of Hughes, Jr. so that it permits efficient and cost effective use of memory to achieve optimal program storages and performance.

As per claim 2, Hughes, Jr. further discloses a typical test system of the type utilized to test integrated circuit board. Such test system, usually referred to as "incircuit" testers (col. 2, lines 58-61). Regelman further discloses wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins (test points/channels) of a tester to execute the test vectors for the pin (col. 4, lines 5-20) and wherein determining a required memory comprises counting the number of test vectors (a vector counter 506) for each test in the test file. Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the step of counting the number of vectors for each test in the test file to determine a required memory needed for each of a plurality of pins of the integrated circuit as taught by Regelman into the integrated circuit that is mounted to the printed circuit board of Hughes, Jr. to determine a required memory for each circuit board of a tester to execute the test vectors for the board.

As per claim 3, Regelman et al further disclose wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins (test points/channels and a vector counter (506)) of a tester to execute the test vectors for the pin (col. 4, lines 5-20).

As per claim 4, Regelman et al further disclose wherein determining a required memory comprises counting the number of test vectors (a vector counter 506) for each test in the test file.

As per claim 5, the teaching of Hughes, Jr. and Regelman have been discussed above. Hughes, Jr. further discloses loading the test vectors requires that the individual pin memories containing the test vector be loaded in one and only one sequence, i.e., the first pin memory is loaded, then the second pin memory is loaded...(col. 4, lines 60-65). Regelman et al further discloses in order to properly test larger memory the tester must be equipped with a significant amount of memory to properly store all of the test vectors that comprises a single test program (col. 2, lines 21-47) and Regelman also discloses a vector counter (506). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to use the vector count (506) of Regelman to count test vectors that is loaded to the first pin of memory of Hughes, Jr. to determine a required memory for the first pin and set the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement in order to properly test larger memory with a significant amount of memory to properly store all of the test vectors that comprises a single test program.

As per claim 6, this claim is rejected under similarity as set forth in claim 5.

As per claim 7, Regelman et al further disclose if the required memory exceeds an existing memory allotment, increasing the allotment of memory (col. 2, lines 31-34. and col. 20, lines 50-54).

As per claims 8-9, the teaching of Hughes and Regelman et al have been discussed above. They do not disclose if the required memory exceeds an existing memory allotment, notifying a user of an amount of additional memory required. However, Regelman et al disclose checking if the required memory exceeds an existing memory allotment (col. 13, lines 17-23, col. 16, lines 5-10) and Regelman et al also disclose if additional software units are required, the memory management process communicates to the user that one or more necessary software are not available. The user then determines which new test file is required (col. 20, lines 1-27). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to set the memory management process to notify the user of an amount of additional memory required if the required memory exceeds an existing memory allotment so that the user can provides sufficient memory space as test pattern increase in size in order to accommodate the entire test program.

As per claim 10, this claim is rejected under similar rationale as set forth in claim 1.

As per claim 11, this claim is rejected under similar rationale as set forth in claim 2.

As per claim 12, this claim is rejected under similar rationale as set forth in claim 3.

As per claim 13, this claim is rejected under similar rationale as set forth in claim 4.

As per claims 14-15, these claims are rejected under similar rationale as set forth in claims 8-9.

As per claim 16, Hughes and Regelman et al do not specifically disclose using the required memory to bill a customer. However, Regelman et al disclose determining a required memory needed to execute the plurality of test vectors (col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5, col. 15, lines 50-67 to col. 16, lines 1-10, col. 19, lines 47-67 to col. 20 lines 1-27). Regelman et al further disclose that non-volatile memory manufacturers that sell to the electronic equipment manufacturers require testers to exercise and verify the proper operation of the memories that they produce. Due to the volume of non-volatile memories that are manufactured and sold at consistently low prices, it is very important to minimize the time it takes to test a single part (col. 1, lines 21-34). Non-volatile memory manufacturers have responded to many of the testing issues by building special test modes into the memory devices. These test modes are not used at all by the purchaser of the memory, but may be accessed by

the manufacturer to test all or significant portions of the memories in as little time as possible and as efficiently as possible (col. 1, lines 43-49). Therefore, it would have been obvious to a person of skilled in the art, at the time the invention was made, based on the determining of the required memory needed to execute the plurality of test vectors, the manufacturers would use the required memory, when desired if needed, to bill a customer (purchaser).

(10) Response to Argument

Appellant argues with respect to claims 1, 7-10, 14 & 15:

With respect to claim 1, the Examiner admits that Hughes fails to disclose "determining a required memory to execute [a] plurality of test vectors". However, the Examiner asserts that Regelman teaches this in col. 2, lines 21-24 & 31-34, and in col. 2, line 60 to col. 3, line 5. Appellant respectfully disagrees.

The excerpts of Regelman referenced by the Examiner state:

In order to properly test larger memories the tester must be equipped with a significant amount of memory to properly store all of the test vectors that comprise a single test program. Col. 2, lines 21-24.

As test programs increase in size, a natural solution is to merely increase the amount of embedded SRAM in order to accommodate the entire test program.

Col. 2, lines 31-34.

A method for managing execution of a program, wherein the program initiates execution of one or more patterns and one or more of the patterns

depend upon one or more software units, downloads a test file into a secondary memory. The test file contains the patterns and the software units that are downloaded into the secondary memory. The process then initiates execution of a called pattern from the available patterns and determines dependencies of the called pattern. The process allocates space in a primary memory for the called pattern and the dependencies. The called pattern and the dependencies are then selectively copied from the secondary memory to the primary memory prior to executing the called pattern. (See col. 2, line 60 to col. 3, line 5)

Although the Examiner matter-of-factly asserts that Regelman teaches "determining a required memory needed to execute [a] plurality of test vectors", the above excerpts from Regelman do not teach or suggest this. If anything, the above excerpts (and Regelman as a whole) teach away from "determining a required memory needed to execute [a] plurality of test vectors". Instead, Regelman merely states the "brute force" solution that a tester "must be equipped with a significant amount of memory to properly store all of the test vectors" and "a natural solution is to merely increase the amount of embedded SRAM in order to accommodate the entire test program".

Examiner disagrees with appellant because Regelman discloses the process allocates space in a primary memory for the called pattern and the dependencies. The called pattern and the dependencies are then selectively copied from the secondary memory to the primary memory prior to executing the called pattern (see col. 2, lines

21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5) to determine a required memory needed to execute a plurality of test vectors or making sure there is a significant amount of memory needed to execute a plurality of test vectors. Regelman also disclose that the memory management process determines if there is sufficient room in the primary memory to copy the additional software units such as the new called test pattern and any additional algorithmic subroutines. (See col. 15, lines 50-67 to col. 16, lines 1-10, col. 19, lines 47-67 to col. 20 lines 1-27). Therefore, the rejection of claims 1, 7-10, 14 & 15 is maintained.

Appellant argues that Regelman fails to indicate how one determines how much memory to add, or what happens if there is not enough memory. Instead, Regelman only indicates that a tester better have a "significant amount" of memory to make sure that everything works.

Examiner disagrees because appellant argument is directed to the specification but not to the claim.

Appellant also argues with respect to claims 1, 7-10, 14, & 15:

> In the last of the preceding excerpts from Regelman, Regelman indicates that, "The process allocates space in a primary memory for the called pattern and the dependencies." Yet, once again, Regelman does not indicate that any determination is made regarding "a required memory needed to execute [a] plurality of test vectors." Presumably, Regelman merely uses the "brute force" approach of making sure there is a "significant amount" of memory.

Of course, Regelman could certainly be modified to implement the method of claim 1. However, appellant cannot find any teaching or suggestion to do this in the art of record.

Examiner disagrees with appellant because the process of allocating space in a primary memory for the called pattern and the dependencies is to determine a required memory needed to execute a plurality of test vectors or making sure there is a significant amount of memory needed to execute a plurality of test vectors.

Appellant argues:

In the past, and given that Regelman does not teach or suggest a step of "determining a required memory needed to execute [a] plurality of test vectors", the Examiner has asserted that it is "inherent" that Regelman's system would need to do this. See, e.g., the 1/31/2007 Final Office Action, p. 2, Sec. 3.a. However, appellant disagrees. Appellant notes that there are other ways of dealing with a plurality of test vectors that exceed the storage limitations of a memory. For example, Regelman could attempt to load a plurality of test vectors into memory. If the test vectors do not fit within the memory, a failure could be indicated, and a user could then add a more "significant amount" of memory and try once again to load the test vectors. Alternately, a user could simply purchase significantly more memory than what he believes is needed, to make sure that the storage requirements of a plurality of test vectors never exceed the size of a tester's memory.

As a result of there being other ways to deal with the problem of a plurality of test vectors exceeding the size of available memory, appellant does not believe it is "inherent" that Regelman must "determine" any sort of "required memory needed to execute a plurality of test vectors. This being the case, appellant asserts that Regelman does not teach the step of "determining a required memory needed to execute the plurality of test vectors", and appellant's claim 1 should be allowed over Regelman's teachings.

Examiner disagrees with appellant because appellant's argument is based on the office rejection dated 1/31/07 but not directed to the office rejection dated 1/31/08 which is now on appeal.

Therefore, the rejection of claims 1, 7-10 and 14-15 is maintained.

Appellant argues with respect to claims 2-4:

With respect to claims 2-4, the Examiner asserts that Regelman teaches "determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board" (where the Examiner deems Regelman's integrated circuit wafers as "boards of a tester"); "determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin" (col. 4, lines 5-20); and "counting the number of test vectors for each test in the test file" (col. 2, lines 21-24 and col. 4, lines 42-43). However, although the Examiner has attempted to correlate elements of

appellant's claims with elements of Regelman's teachings, the Examiner has not shown where Regelman teaches "determining the required memory" needed for these elements to execute a plurality of test vectors. This is because Regelman contains no such teaching.

Furthermore, and with respect to claim 2's step of determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board, one of ordinary skill in the art would certainly not equate an "integrated circuit wafer" with a "board of a tester". That is, an integrated circuit wafer might be the "device" to which vectors are applied (see claim 1), but an integrated circuit wafer is not a "board of a tester".

Examiner disagrees with appellant because the teaching of Huges, Jr. and Regelman have been discussed above. Hughes, Jr. further discloses a typical test system of the type utilized to test integrated circuit board. Such test system, usually referred to as “incircuit” testers (col. 2, lines 58-61). Regelman further discloses wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins (test points/channels) of a tester to execute the test vectors for the pin (col. 4, lines 5-20) and wherein determining a required memory comprises counting the number of test vectors (a vector counter 506) for each test in the test file. Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the step of counting the number of vectors for each test in the test file to determine a required memory needed for each

of a plurality of pins of the integrated circuit as taught by Regelman into the integrated circuit that is mounted to the printed circuit board of Hughes, Jr. to determine a required memory for each circuit board of a tester to execute the test vectors for the board.

Appellant argues with respect to claim 4, nowhere does Regelman mention or suggest "counting" or a "counter".

Examiner disagrees with appellant because Regelman does disclose a vector count (506). (See col. 15, line 62).

Therefore, the rejection of claims 2-4 and 11-13 are maintained.

Appellant argues with respect to claims 5 & 6:

Claim 5 recites a very specific method for "determining a required memory needed to execute a plurality of test vectors". The method involves 1) determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file, and then 2) setting the required memory equal to the first memory requirement. Thereafter, and for each additional pin of a tester, 1) a second memory requirement needed for the additional pin to execute the test vectors for the first test is determined, and 2) if the second memory requirement is greater than the first memory requirement, the required memory is set to the second memory requirement.

Although the Examiner asserts that Regelman's col. 20, lines 50-54, teach the method set forth in claim 5, this excerpt contains no such teaching. Rather, this

excerpt is directed to a process of overwriting memory when memory is unavailable. Nowhere does Regelman teach that the amount of memory required "to execute a plurality of test vectors" is determined.

Examiner disagrees with appellant because the teaching of Hughes, Jr. and Regelman have been discussed above. Hughes, Jr. further discloses loading the test vectors requires that the individual pin memories containing the test vector be loaded in one and only one sequence, i.e., the first pin memory is loaded, then the third pin memory is loaded...(col. 4, lines 60-65). Regelman et al further discloses in order to properly test larger memory the tester must be equipped with a significant amount of memory to properly store all of the test vectors that comprises a single test program (col. 2, lines 21-47) and Regelman also discloses a vector counter (506). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to use the vector count (506) of Regelman to count test vectors that is loaded to the first pin of memory of Hughes, Jr. to determine a required memory for the first pin and set the required memory equal to the first memory requirement; and for each additional pin of the tester, determining a second memory requirement needed for the additional pin to execute the test vectors for the first test;

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement in order to properly test larger memory with a significant amount of memory to properly store all of the test vectors that comprises a single test program.

Therefore, the rejection of claim 6 is maintained.

Appellant argues with respect to claim 16:

The Examiner asserts that Regelman teaches "using the required memory to bill a customer" (col. 2, lines 21-24 & 31-34, and col. 2, line 60 - col. 3, line 5). Appellant respectfully disagrees.

All that Regelman discloses is that memory is "costly". This simple observation does not teach or suggest that a customer should be billed based on a "required memory" needed to execute a plurality of test vectors.

The Examiner further asserts that it would have been obvious to bill a user for "required memory". However, the Examiner has not provided any evidence to support this assertion.

Examiner disagrees with appellant because the teaching of Hughes and Regelman et al have been discussed above. They do not specifically disclose using the required memory to bill a customer. However, Regelman et al disclose determining a required memory needed to execute the plurality of test vectors (col. 2, lines 21-24, lines 31-34, lines 60-67 to col. 3, lines 1-5, col. 15, lines 50-67 to col. 16, lines 1-10, col. 19, lines 47-67 to col. 20 lines 1-27). Regelman et al further disclose that non-volatile memory manufacturers that sell to the electronic equipment manufacturers require testers to exercise and verify the proper operation of the memories that they produce. Due to the volume of non-volatile memories that are manufactured and sold at

consistently low prices, it is very important to minimize the time it takes to test a single part (col. 1, lines 21-34). Non-volatile memory manufacturers have responded to many of the testing issues by building special test modes into the memory devices. These test modes are not used at all by the purchaser of the memory, but may be accessed by the manufacturer to test all or significant portions of the memories in as little time as possible and as efficiently as possible (col. 1, lines 43-49). Therefore, it would have been obvious to a person of skilled in the art, at the time the invention was made, based on the determining of the required memory needed to execute the plurality of test vectors, the manufacturers would use the required memory, when desired if needed, to bill a customer (purchaser).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

//Phung M. Chung//
Primary Examiner, Art Unit 2117

Conferees:

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117

/RWB/
Supervisor Patent Examiner: Robert Beausoliel, Jr.